Nanometer-scale patterning and individual current-controlled lithography using multiple scanning probes

Kathryn Wilder, a) Hyongsok T. Soh, Abdullah Atalar, b) and Calvin F. Quate
E. L. Ginzton Laboratory, Stanford University, Stanford, California 94305-4085

(Received 3 September 1998; accepted for publication 19 March 1999)

Scanning probe lithography (SPL) is capable of sub-30-nm-patterning resolution and nanometer-scale alignment registration, suggesting it might provide a solution to the semiconductor industry’s lithography challenges. However, SPL throughput is significantly lower than conventional lithography techniques. Low throughput most limits the widespread use of SPL for high resolution patterning applications. This article addresses the speed constraints for reliable patterning of organic resists. Electrons field emitted from a sharp probe tip are used to expose the resist. Finite tip-sample capacitance limits the bandwidth of current-controlled lithography in which the tip-sample voltage bias is varied to maintain a fixed emission current during exposure. We have introduced a capacitance compensation scheme to ensure continuous resist exposure of SAL601 polymer resist at scan speeds up to 1 mm/s. We also demonstrate parallel resist exposure with two tips, where the emission current from each tip is individually controlled. Simultaneous patterning with multiple tips may make SPL a viable technology for high resolution lithography. © 1999 American Institute of Physics. [S0034-6748(99)04906-0]

I. INTRODUCTION

Scanning probe lithography (SPL) may be used to pattern nanometer-scale features on a variety of substrates.1–3 In fact, scanning probes have been used to manipulate individual atoms, achieving perhaps the ultimate lithographic resolution.4,5 However, the serial nature of SPL makes this technology much slower than “mask” techniques such as photolithography, x-ray lithography, or extreme ultraviolet (EUV) lithography. A potential advantage of a direct write approach is that it does not require expensive and time-consuming mask fabrication. SPL may also have superior alignment capabilities. Nevertheless, in order for SPL to become a viable technique for high resolution lithography, the throughput must be dramatically increased. We believe SPL throughput can be increased by attacking the issue on two fronts: (1) by increasing the writing speed with a single tip and (2) by patterning simultaneously with multiple probes.

We have previously shown that operating in the hybrid atomic force microscope (AFM)/scanning tunneling microscope (STM) lithography mode has several advantages over other SPL techniques.6 In this mode, both the tip-sample force and the emission current are independently controlled for resist exposure. The tip is held in contact with the resist surface to minimize beam spreading for enhanced patterning resolution. A voltage bias between the probe and the sample generates the field emission of electrons from the sharp probe tip. The voltage is varied to maintain a constant emission current. The current feedback ensures that a constant dose of electrons is delivered to the resist, yielding uniform lithography even when the resist thickness varies as a function of position. This method has since been adopted by other groups because of the improved performance and reliability.7,8 The lithographic speed is limited primarily by the bandwidth of the feedback loops used to control force and current. In Sec. II we demonstrate increased patterning speed where electrons emitted from the tip are used to expose the resist.

Further increases in patterning throughput require simultaneous writing with multiple probes. Minne et al. performed parallel oxidation lithography with an array of cantilevers.9 Since the electric-field-enhanced oxidation process is inherently slow, it may not be suitable for high throughput patterning. In Sec. III we address the challenges encountered when the resist exposure scheme is extended to multiple tips with individual control of the current from each tip.

II. HIGH SPEED PATTERNING WITH A SINGLE TIP

A. Control of the tip-sample force

The mechanical response of the actuator that moves the probe up and down limits the scan speed with constant force maintained. Generally, the piezotube scanner is used as the actuator. This large device typically has a resonance below 1 kHz, limiting the scan speed to below 200 μm/s. Manalis et al. demonstrated that the tip velocity can be increased by at least an order of magnitude by using a piezoelectric actuator integrated onto the cantilever.10 Minne et al. have used such cantilevers for high speed imaging with multiple tips where the tip-sample force was maintained simultaneously and independently by each cantilever.11,12

As a simpler alternative, we have investigated the feasibility of performing exposure lithography in the constant-height AFM mode, where the tip is scanned in contact with the sample without controlling the tip-sample force. Minne et al. found that the quality of oxidation lithography was

a)Electronic mail: kwilder@leland.stanford.edu
b)Present address: Bilkent University, Ankara, Turkey 06533.
higher with constant force maintained. The higher forces between the tip and hard silicon sample apparently damaged the tip and degraded patterning fidelity. Because the surface of an organic resist is soft and pliable, we do not expect small variations in the applied force to damage the tip. However, excessive force between the tip and sample could cause the tip to penetrate (or scratch) the resist.

We have tested exposure lithography with and without real-time force feedback. For constant-height scanning, we lowered the tip toward the resist-coated sample until the cantilever was deflected slightly (~10 nN force between the tip and resist). The tip was then moved in the x-y plane of the sample and the current feedback was enabled. Figure 1 shows that lines written with and without force feedback appear to have equivalent fidelity. In fact, in some instances patterns written in the constant height mode had superior uniformity. The tip-sample bias used to generate the electron beam contributes an electrostatic force that has an adverse effect on the force feedback. We observed this effect as a variation in voltage during lithography on flat samples; the voltage is generally more steady in the constant height mode. If the cantilevers were sufficiently compliant, this constant-height scanning scheme should also work for patterning over topography. Therefore either by incorporating integrated actuators or by operating in the constant height AFM mode, the lithography speed is not limited by the response of the force feedback. Maintaining the emission current (or exposure dose) at a fixed level during lithography at high scan speeds is the remaining challenge.

B. Control of the emission current

Our current control system varies the tip-sample voltage bias (HV) to maintain a fixed emission current. The effective bandwidth of the current feedback is limited by the presence of a finite tip-sample capacitance, C_{t-s}. A change in voltage generates a displacement current proportional to C_{t-s}. Therefore the total measured current (I_{meas})—which the feedback ties to keep constant—is a sum of the exposing current through the resist (I_{res}) and the capacitive current (I_{cap})

\[ I_{meas} = (I_{res} + I_{cap}) = I_{res} + C_{t-s} \frac{\partial HV}{\partial t}, \]

assuming a constant C_{t-s}.

We have measured a probe-sample capacitance as high as 2.4 pF, which is mostly due to the chip (3.6 mm × 1.6 mm) on which the cantilever and tip are fabricated. We previously reported that by reducing the size of this chip to a width of about 0.4 mm we could reduce the capacitance to below 600 fF. Figure 2 shows the effect of the chip size on the voltage ramp during current-controlled lithography. The setpoint current was abruptly changed from 0 to 50 pA at time \( t = 0.3 \) s. Curve (a) shows a voltage ramp of 30 V/s for the full chip (measuring 3.6 mm in width). The measured capacitance is 1.7 pF. Curve (b) corresponds to the chip shown above that has been reduced to about 0.4 mm in width. The voltage here ramps at 91 V/s, indicating the capacitance has been reduced to 550 fF.

In order to further reduce the influence of the probe-sample capacitance, we build a circuit that compensates for the capacitive component of the current and ensures that the
feedback responds primarily to the exposing current [Fig. 3(a)]. The compensation circuit generates a voltage proportional to the displacement current:

\[ V_{\text{comp}} = R_{\text{comp}} C_{\text{comp}} \frac{\partial HV}{\partial t}. \]  

(2)

\( V_{\text{comp}} \) is subtracted from the output of the current preamplifier \( V_{\text{meas}} \) to yield a voltage proportional to the current through the resist \( V_{\text{res}} \):

\[ V_{\text{res}} = (V_{\text{meas}} - V_{\text{comp}}) = S I_{\text{meas}} - R_{\text{comp}} C_{\text{comp}} \frac{\partial HV}{\partial t}. \]  

(3)

where \( S \) is the gain of the current preamplifier in units of V/A. The current control then feeds back on \( V_{\text{res}} \), thus maintaining a constant exposing current through the resist.

\( C_{\text{comp}} \) was chosen smaller than the probe-sample capacitance, although its precise value is not important since the compensation may be matched to the capacitance of a given system by adjusting \( R_{\text{comp}} \). Figure 3(b) shows the effect of \( R_{\text{comp}} \) on the voltage ramp. Here the setpoint current was changed abruptly from 0 to 80 pA at time \( t = 5 \) s. In all cases the feedback immediately responded, making the measured current equal to the setpoint current. With no compensation \( (R_{\text{comp}} = 0) \), the voltage increased slowly (122 V/s), corresponding to a tip-sample capacitance of 820 fF. For approximately 0.5 s there was no exposure. At a slow scan speed of 0.1 \( \mu \)m/s, this corresponds to a scan distance of only 50 nm; at a high scan speed of 1 mm/s, there is no patterning until the tip has traveled 0.5 mm, and this is clearly unacceptable. The voltage ramp can be dramatically increased by adjusting \( R_{\text{comp}} \) [Fig. 3(b)]. The fastest voltage ramp shown here is 1160 V/s, corresponding to an effective capacitance of 85 fF. The effective capacitance may be further minimized by fine-tuning \( R_{\text{comp}} \), although it can never be completely eliminated and therefore continues to limit the response of the current feedback.

C. Lithography

The reduced effective capacitance allows the current feedback to keep the exposing current constant even at high scan speeds. We used this system to pattern Microposit SAL601 negative tone resist at scan speeds from 1 \( \mu \)m/s to 1 mm/s with various current setpoints. Silicon samples were prepared by etching off the native oxide, singeing, and priming with vapor hexamethyldisilazane (HMDS) adhesion promoter prior to spin coating the resist. Details are given in Ref. 6. After exposure, the wafer was given a postexposure bake (PEB) for 1 min at 115 °C and developed in MF-322 for 10 min. Figure 4 shows a scanning electron microscope (SEM) image of lines patterned in 65-nm-thick resist at a scan speed of 0.5 mm/s and an emission current of 1 nA. The linewidth is approximately 65 nm. The SEM image was taken after dry etch pattern transfer into the silicon substrate. The lines are on a 500 nm pitch and were exposed with an emission current of 1 nA. The linewidth is approximately 65 nm.

The voltage required to emit a given current depends strongly on both the scan speed and the re-
sist thickness. Figure 5(a) shows the tip-sample voltage bias necessary to achieve a setpoint current of 20, 50, and 100 pA at various scan speeds (solid lines). Constant force was maintained between the probe and the surface of a 65-nm-thick SAL601 resist film. At higher scan speeds, a higher voltage is required to maintain a given emission current. The tip-sample voltage dependence on scan speed is due to stress in the resist resulting from the high dose applied to the tip. In either case, the tip and sample are clearly coupled. Herein lies the challenge for multiple tip lithography because of this strong dependence of emission on resist thickness and scan speed.

III. CURRENT-CONTROLLED LITHOGRAPHY WITH TWO TIPS

We have demonstrated dramatic improvements in the writing speed with a single tip. However, patterning throughput (generally quoted in wafers per hour) is still too low to make SPL a viable large-scale patterning technology. We envision a higher-throughput lithography system in which multiple probes pattern simultaneously, all scanning at speeds above 1 mm/s. In order to maintain the patterning reliability of our single tip system, we require individual control of the emission current from each tip. The current feedback system used for a single tip draws the current to the preamplifier’s virtual ground at the tip and applies a positive voltage to the sample. Alternatively, the current may be measured at the sample (at ground) while a negative bias is applied to the tip. In either case, the tip and sample are clearly coupled. Herein lies the challenge for multiple tip lithography.

In order to enable independent control of the emission current from multiple tips, we need a system capable of measuring the current at each tip and applying a high voltage to each tip. The sample, shared by all tips, must be held at a fixed voltage. Figure 7(a) depicts this scheme. The high volt-
average current preamplifier measures the current flow from tip to sample by precisely measuring the voltage drop across a large reference resistor. The circuit design, based on the instrumentation amplifier configuration, was chosen because of its high input impedance and its high common mode rejection ratio (CMRR). We designed and built a two-channel current preamplifier capable of low-noise current measurements at high voltages. Figure 7(a) shows a circuit diagram of one channel. All operational amplifier stages are high voltage devices. Device U2 in particular must have an extremely high input impedance and low bias currents since its noninverting input is in parallel with the tip/resist system. We use the Apex Microtechnology high power FET input amplifier PA85 for U1 and U2, and Apex’s PA87A for U3, U4, and U5. The circuit gain is controlled by the ratio $R_2/R_1$ and can be varied without affecting the input impedance or the circuit CMRR:

$$V_{\text{meas}} = (V_1 - V_2) = \left(1 + \frac{2R_2}{R_1}\right)(V_{\text{tip}} - HV) = \left(1 + \frac{2R_2}{R_1}\right)R_{\text{ref}}I.$$  \hspace{1cm} (5)

The sensitivity of the high voltage preamplifier is $10^9$ V/A. The minimum detectable current is set by the size of the reference resistor ($R_{\text{ref}}$). We have selected a 100 MΩ, 1% tolerant precision resistor for $R_{\text{ref}}$. The preamplifier therefore provides accurate measurements from 50 pA to 10 nA, which spans the appropriate current range for SPL. The high voltage preamplifier has a CMRR of almost 90 dB.

The cable capacitance and the input capacitance of U2 are in parallel with the tip-resist system, compounding our previous capacitance problem. We could compensate for these additional capacitances as described in Sec. II. However, since their magnitude far exceeds the original tip-sample capacitance, we cannot expect to reduce the effective capacitance to tolerable levels in this way. Here we show an alternative technique for minimizing the effect of these capacitances. First, we use a triaxial cable between the tip and the preamplifier, where a guard driver is used to raise the cable guard to the tip voltage. Second, we employ a boot-
strap technique to minimize the 4 pF input capacitance of U2.\textsuperscript{16} The potentiometer is varied to force the current across an external capacitor ($C_i$) to be equal (and opposite) to the current across the op amp internal input capacitance. Since the input capacitance is somewhat nonlinear, its influence could not be completely eliminated. This capacitance most limits the bandwidth of the current feedback system.

The two-channel current preamplifier was used in conjunction with two identical analog feedback circuits to perform independent current-controlled lithography with two tips. The integral feedback circuit compares the measured current to the setpoint current and varies $HV$ to minimize the error signal. The current setpoint was enabled with a voltage signal from the computer that controls the movement of the probe in order to synchronize the lithography with the tip motion. The current setpoint can be specified independently for each tip.

The cantilevers used were 2×1 arrays of micromachined silicon tips fabricated by Minne and described in Ref. 11. It is important that the two cantilevers are electrically isolated so that the high voltage applied to each tip does not cause significant current flow between the tips. The tips were scanned as a unit along the designated path in the constant height AFM mode. A result of parallel lithography with two tips is shown in Fig. 8, where the pattern on the left was written with tip 1 while the pattern on the right was written simultaneously with tip 2. This current control scheme may be extended to additional tips operating in parallel.

IV. DISCUSSION

We report progress towards higher throughput nanolithography using scanning probes. A compensation circuit was used to minimize the effect of the tip-sample capacitance that limited the effective bandwidth of the current feedback. This allowed us to demonstrate current-controlled lithography of SAL601 resist at speeds up to 1 mm/s. We found that the voltage required to generate the exposing current depends on the tip scan speed and the resist thickness. The exposure line dose was found to be the critical parameter for lithography.

We also extended the current feedback scheme to two tips, where the exposing current from each tip was independently controlled. The independent current feedback allows different setpoint currents to be applied to each tip for individual dose and/or linewidth control. Multiple tip control required a new current preamplifier design with internal capacitance compensation in order to measure currents at high voltages. We demonstrated parallel, current-controlled lithography of SAL601 resist with two tips.

ACKNOWLEDGMENTS

The authors would like to acknowledge the technical contribution of Stanford Professor Tom Lee with respect to the high voltage preamplifier design. K. W. is pleased to acknowledge the financial support of Advanced Micro Devices. This work was supported in part by DARPA under Contract No. MDA972-97-1-0010, by the SRC under Contract No. LC-460, and by ONR.

\textsuperscript{2}E. S. Snow and P. M. Campbell, Appl. Phys. Lett. 64, 1932 (1994).
\textsuperscript{7}H. Sugimura and N. Nakagiri, Nanotechnology 8, A15 (1997).